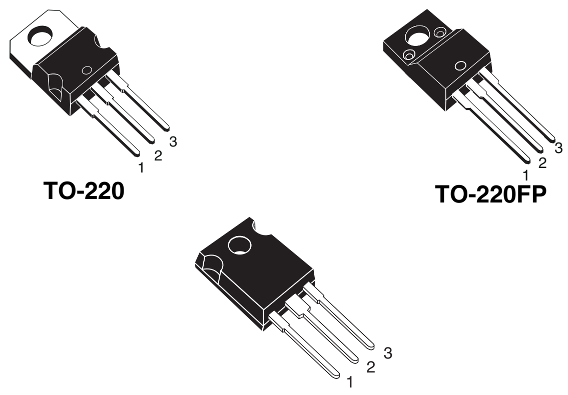
STF13N95K3
STP13N95K3, STW13N95K3

N-channel 950 V, 0.68 Ω, 10 A TO-220, TO-220FP, TO-247 Zener-protected SuperMESH3™ Power MOSFET

Features

Order codes	V_{DSS}	$R_{DS(on)}$max	I_D	P_W
STF13N95K3	950 V	< 0.85 Ω	10 A	40 W
STP13N95K3				190 W
STW13N95K3				

- Gate charge minimized
- Extremely large avalanche performance
- 100% avalanche tested
- Very low intrinsic capacitance
- Zener-protected



Application

Switching applications

Description

These devices are made using the SuperMESH3™ Power MOSFET technology that is obtained via improvements applied to STMicroelectronics' SuperMESH™ technology combined with a new optimized vertical structure. The resulting product has an extremely low on resistance, superior dynamic performance and high avalanche capability, making it especially suitable for the most demanding applications.

Figure 1. Internal schematic diagram

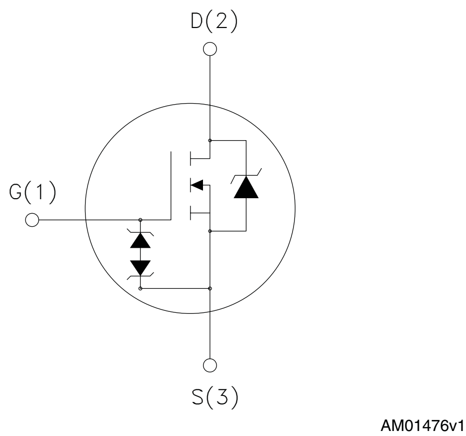


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF13N95K3	13N95K3	TO-220FP	Tube
STP13N95K3		TO-220	
STW13N95K3		TO-247	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, TO-247	TO-220FP	
V_{DS}	Drain source voltage	950		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	10	10 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	6	6 (1)	A
I_{DM} (2)	Drain current (pulsed)	40	40 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	190	40	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	13		A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	400		mJ
dv/dt (3)	Peak diode recovery voltage slope	9		V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	- 55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area.
3. I_{SD} ≤ 10 A, di/dt ≤ 400 A/µs, $V_{Peak} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220	TO-247	TO-220FP	
Rthj-case	Thermal resistance junction-case max	0.66		3.13	°C/W
Rthj-amb	Thermal resistance junction-amb max	62.5	50	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300			°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	950			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating, V_{DS} = max rating,Tc=125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D= 5 A		0.68	0.85	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	1620 117 1.2	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 760 V	-	115	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	131	-	pF
R_G	Intrinsic gate resistance	f = 1MHz open drain	-	2.3	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 760 V, I_D = 10 A V_{GS} =10 V *(see Figure 20)*	-	51 10 30	-	nC nC nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 475 V, I_D = 5 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 22)*	-	18 16 50 21	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)		-		10 40	mA A
V_{SD}(1)	Forward on voltage	I_{SD}= 10 A, V_{GS}=0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 10 A, V_{DD}= 60 V di/dt = 100 A/µs, *(see Figure 21)*	-	500 9 36		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 10 A,V_{DD}= 60 V di/dt=100 A/µs, Tj=150 °C*(see Figure 21)*	-	624 11 37		ns µC A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs ± 1mA, (open drain)	30	-		V

The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP

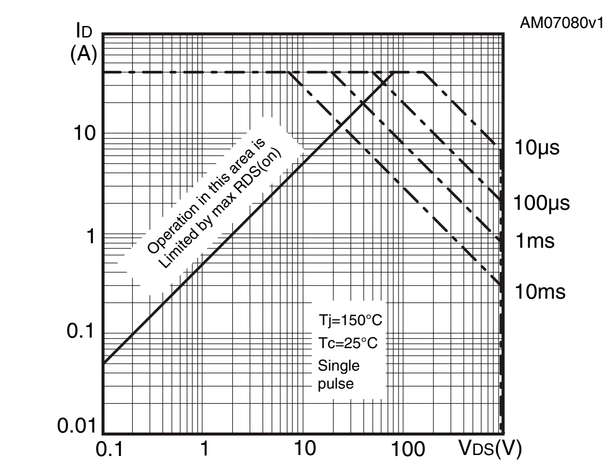


Figure 3. Thermal impedance for TO-220FP

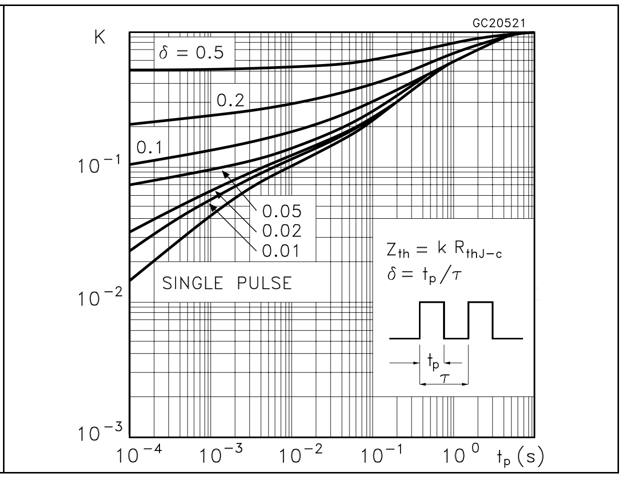


Figure 4. Safe operating area for TO-220

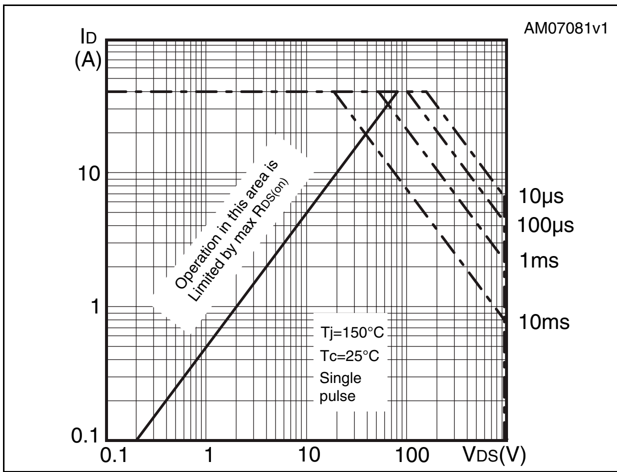


Figure 5. Thermal impedance for TO-220

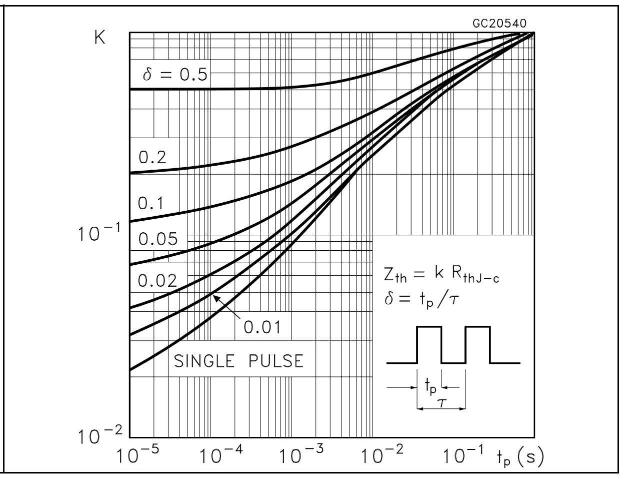


Figure 6. Safe operating area for TO-247

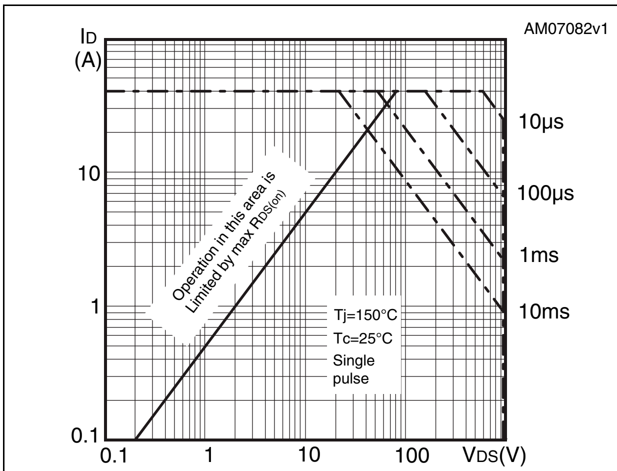


Figure 7. Thermal impedance for TO-247

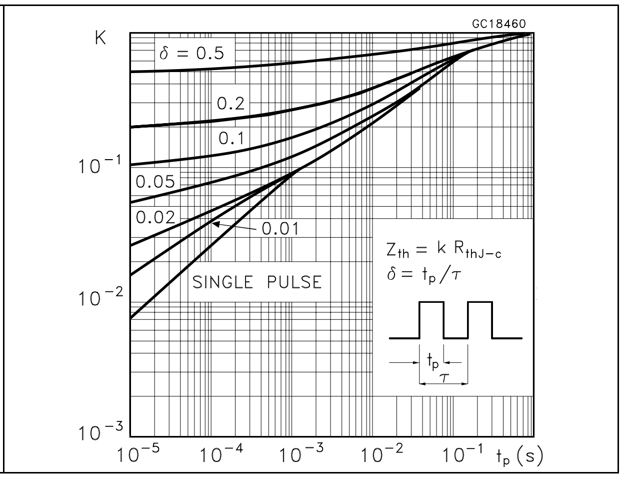


Figure 8. Output characteristics

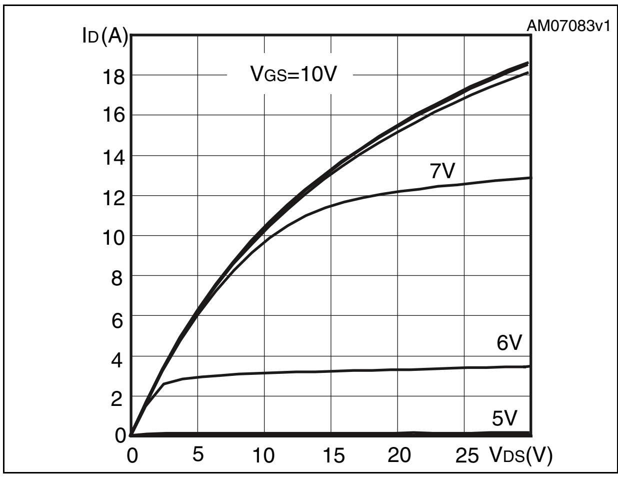


Figure 9. Transfer characteristics

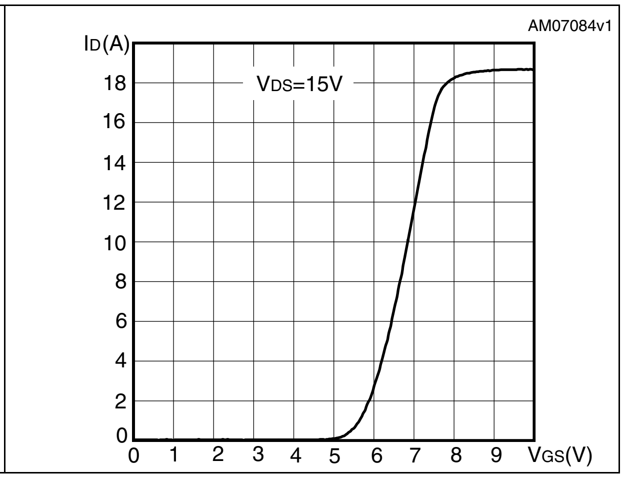


Figure 10. Gate charge vs gate-source voltage

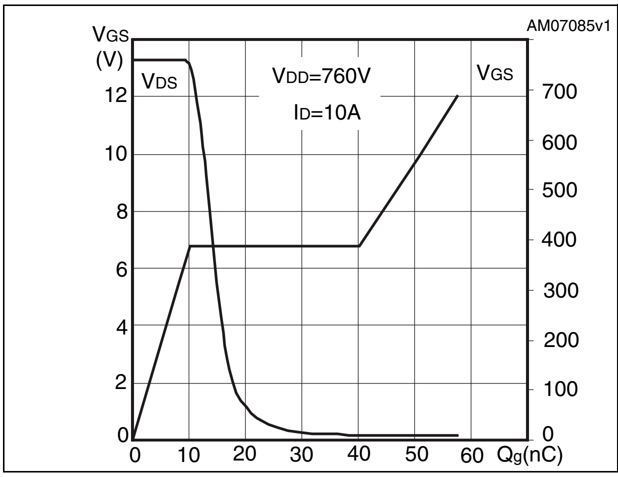


Figure 11. Static drain-source on resistance

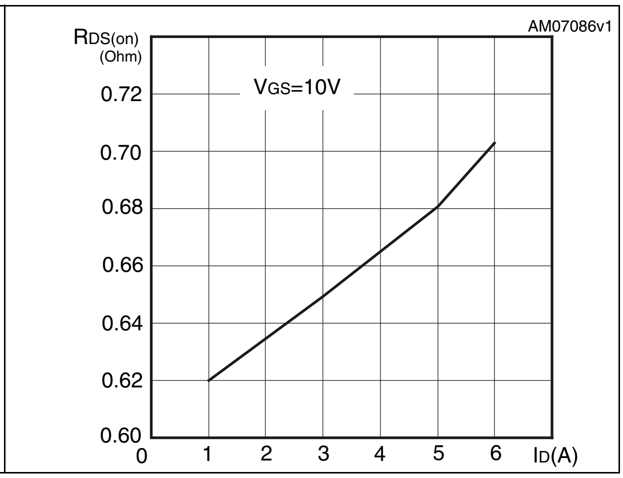


Figure 12. Capacitance variations

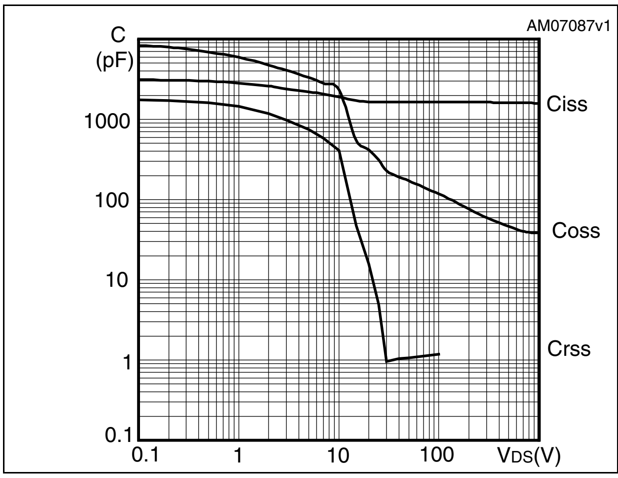


Figure 13. Output capacitance stored energy

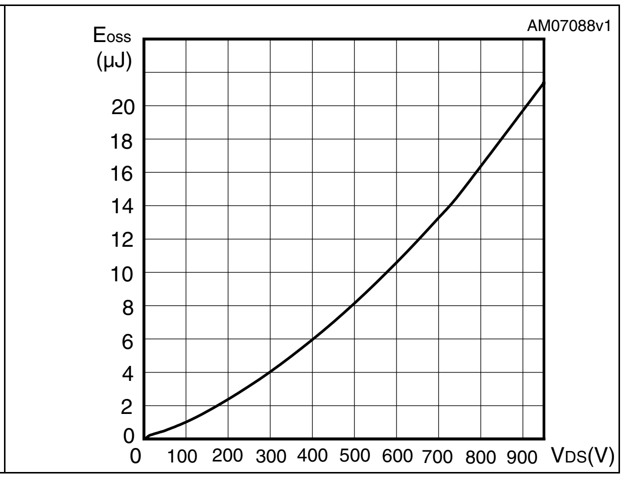


Figure 14. Normalized gate threshold voltage vs temperature

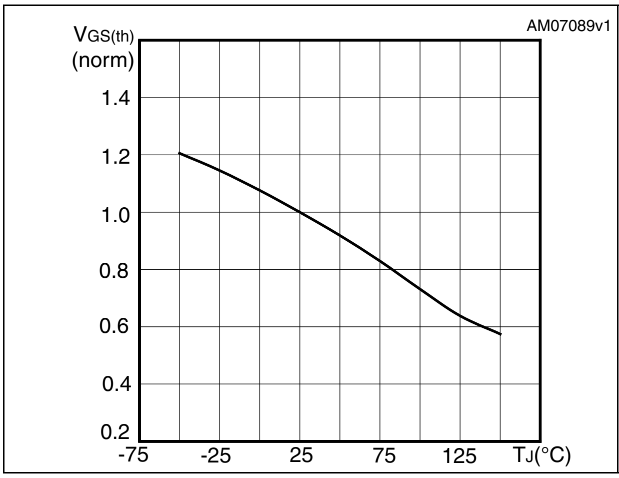


Figure 15. Normalized on resistance vs temperature

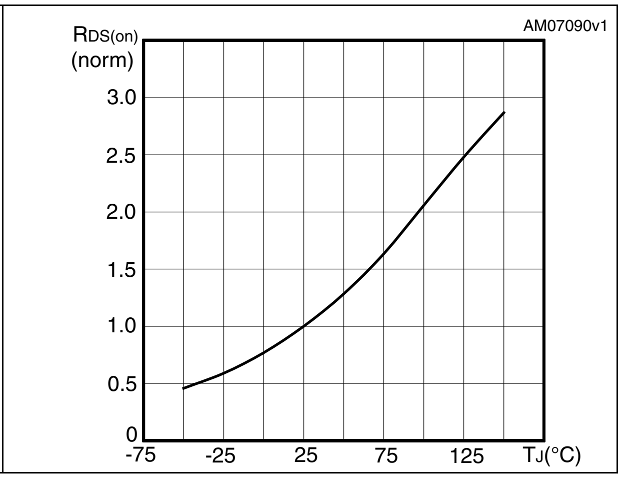


Figure 16. Source-drain diode forward characteristics

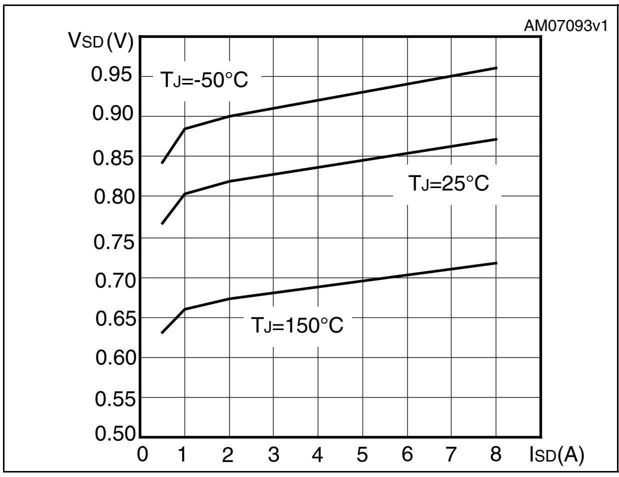


Figure 17. Normalized B_{VDSS} vs temperature

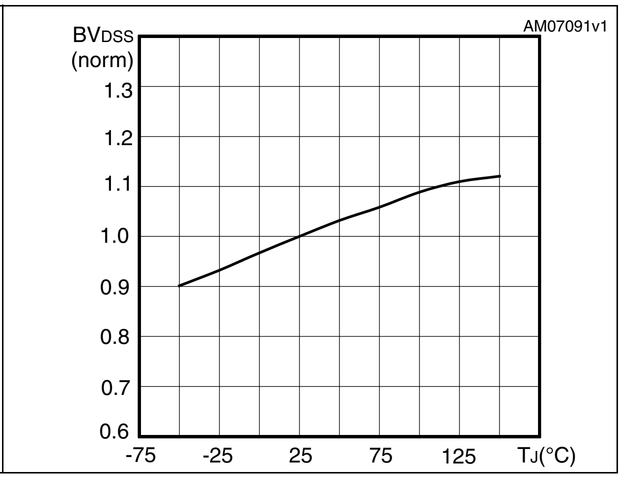
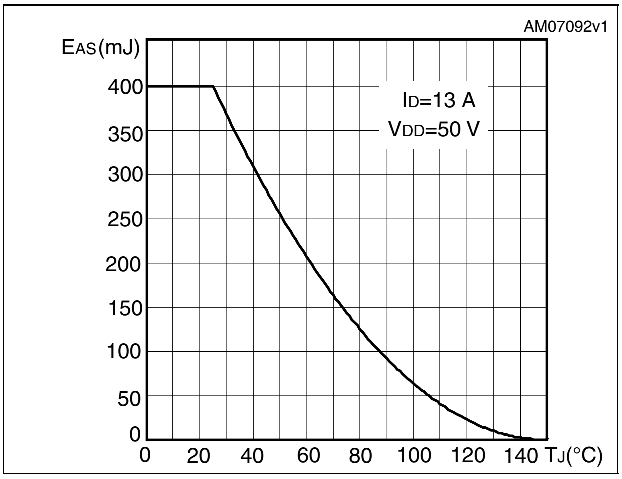


Figure 18. Maximum avalanche energy vs starting Tj



3 Test circuits

Figure 19. Switching times test circuit for resistive load

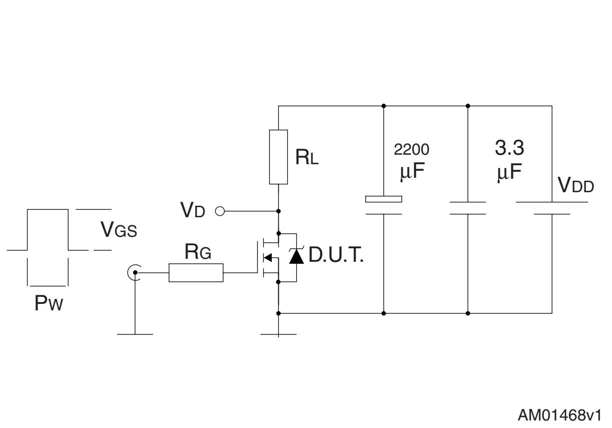


Figure 20. Gate charge test circuit

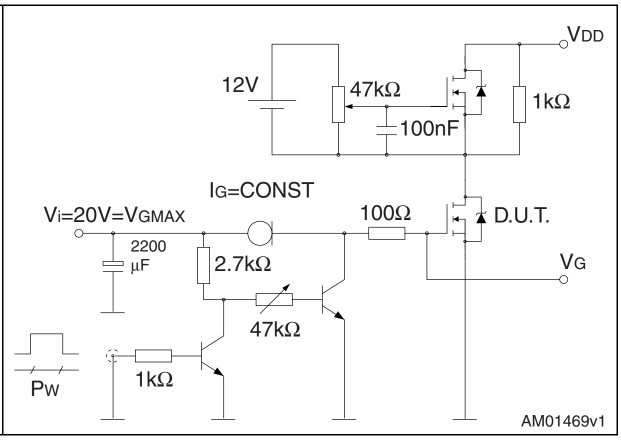


Figure 21. Test circuit for inductive load switching and diode recovery times

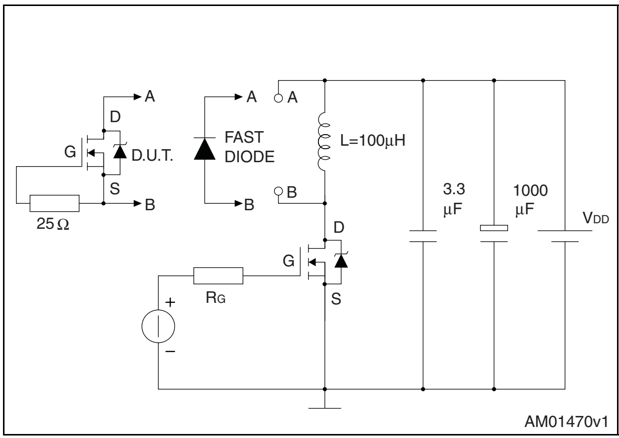


Figure 22. Unclamped inductive load test circuit

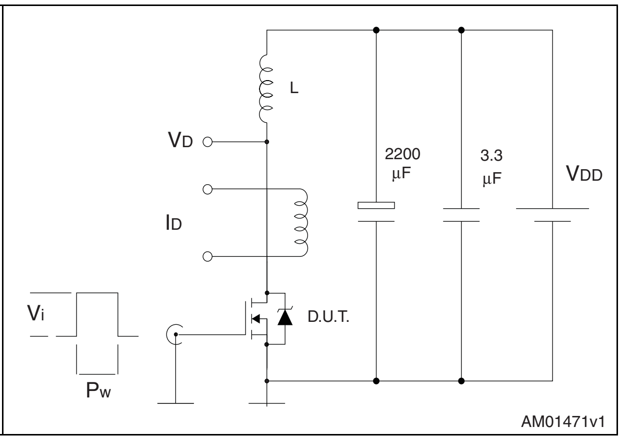


Figure 23. Unclamped inductive waveform

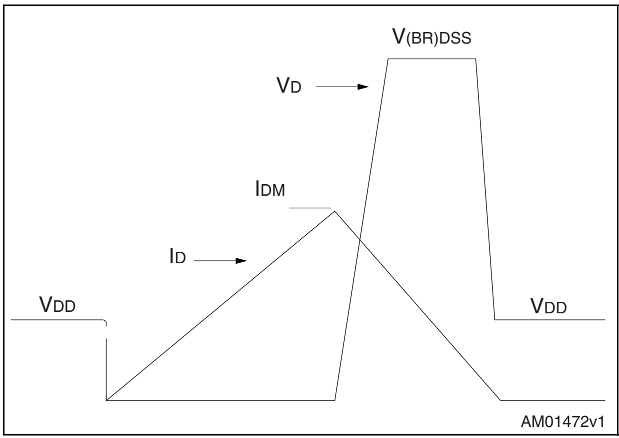
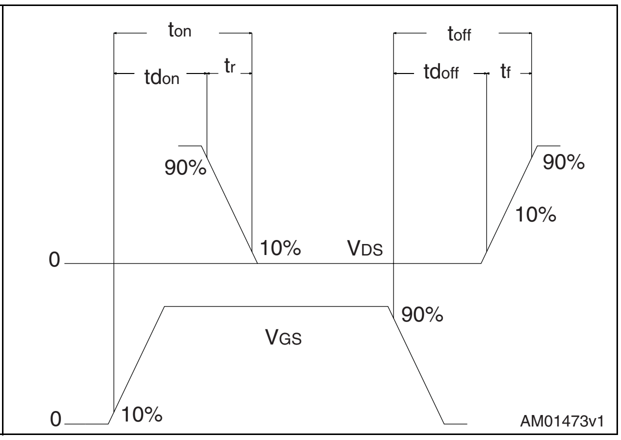


Figure 24. Switching time waveform



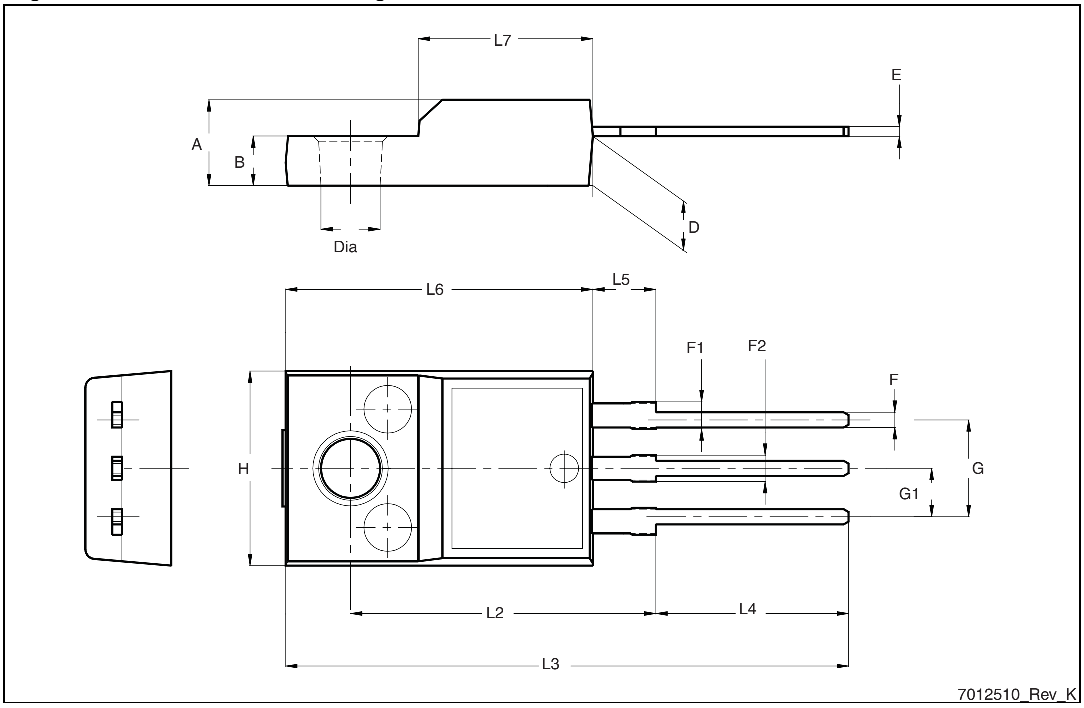
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 9. TO-220FP mechanical data

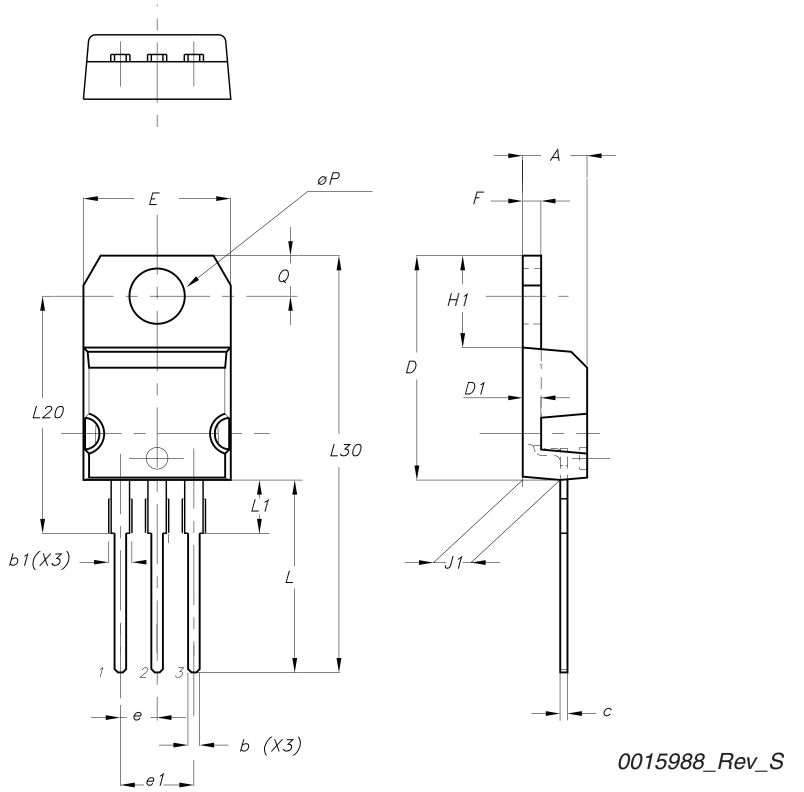
Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 25. TO-220FP drawing



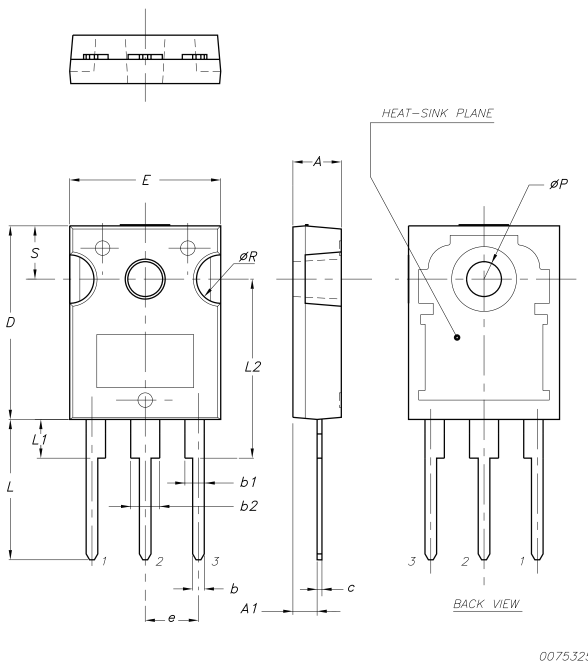
TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95



TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
15-May-2009	1	First release.
02-Sep-2010	2	Document status promoted from preliminary data to datasheet.